EE / CPRE / SE 491 - sdmay20-38
iFPGA - Intermittent Intelligent FPGA Platform
Week7 Report

10/28/19 - 11/1/19
Client: Henry Duwe
Faculty Advisor: Henry Duwe

Team Members:

Jake Tener - Team member, SW focus
Jake Meiss - Team member, HW focus
Andrew Vogler - Team member
Zixuan Guo - Team member
Justin Sung - Team member

Weekly Summary

The goals of this week is to create a comprehensive HW and SW physical and data flow of our system. Prepare materials for the end of semester presentation. Start researching into possible ways upload the SW onto the HW.

Past Week Accomplishments

- HW - Justin Sung, Andrew Vogler, Zixuan Guo
    - Researched into possible ways to support the SW on the HW platform. Based on space and difficulty, we decided that the separate microcontroller possibility had the most promise for success.
        - Linux kernel
        - Separate microcontroller
    - Research attractive IP blocks that can be utilized in the final project. IP's such as a microprocessor, bus controllers, SPI interface, etc.
- Platform/Harvester power analysis - Jake Meiss
    - Tested power consumption and capacitor sizing calculations based off of differing input variables such as output voltage, operating current, and charging/discharging times.
    - Obtained preliminary measurements of the output current of the FPGA running a simple flashing LED program
    - Researched the architecture of both the Igloo Nano and the Powercast in order to understand and take proper measurements
- SW - Jake Tener
    - Created a detailed SW data flow from the input to the eventual output of the NN.
    - Recorded sounds in Durham and ran it through the NN, verifying that everything works as intended.

Pending Issues

- No issues

Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Jake Tener	SW	8	71
Jake Meiss	Platform/Harvester power analysis	8	71
Andrew Vogler	HW	8	71
Zixuan Guo	HW	8	71
Justin Sung	HW	8	71

Plans for Coming Week

- Revise the HW and SW flow further to ensure comprehensive understanding and feasibility
- Timing Breakdown of the SW flow to determine step to accelerate on the HW
- Power analysis, specifically the in-rush and dynamic when all resources are being utilized
- Adder tree simulation to max out resource utilization for power analysis